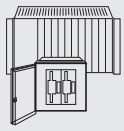
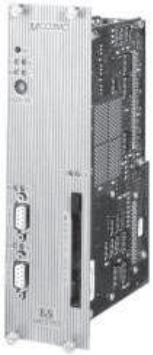


B&R MAESTRO COPROCESSORS

B&R MAESTRO Coprocessors are industrial computers that can be applied universally. By using several coprocessors in one rack (multiprocessor system), the power and efficiency of a B&R MAESTRO system is increased considerably.

MCO1
68000 / 12,5 MHz

MCO3
68030 / 33 MHz



MCO3MC
68030 / 33 MHz

TECHNICAL DATA	MCO1	MCO3	MCO3MC
Processor	68000	68030	68030
Clock frequency	12.5 MHz	33 MHz	33 MHz
Memory Management Unit	-	YES	YES
Arithmetic processor	68881	68882	68882
Operating system	OS-9/68000	OS-9/68030	OS-9/68030
Memory	0.5 MByte SRAM 1 MByte FPROM optional	0.5 MByte SRAM 2 MByte DRAM 1 MByte FPROM	0.5 MByte SRAM 10 MByte DRAM 1 MByte FPROM
Interfaces	RS232/TTY RS232/RS485	RS232/TTY RS232/RS485	RS232/TTY RS232/RS485
PCMCIA Interface	-	-	YES

B&R MAESTRO coprocessors offer all kinds of different configurations. Here are just a few examples:

- as single processors in PLC systems
- as main processors of industrial computer systems
- for multiprocessor systems

AS A SINGLE PROCESSOR IN THE PLC

B&R MAESTRO coprocessors do not have to be components of a B&R MAESTRO system. They can be operated in all P slots of PLC racks without a B&R MAESTRO bus board.

RACK	SLOTS	SUITABLE FOR MCO
ECR165-0 (MULTICONTROL)	16 ($0 to $F)	$0 to $F
MDR085-0 (MIDI)	8 ($0 to $7)	$0 to $7
M2R111 (M264)	11 ($0 to $A)	$0 to $4

The B&R MAESTRO coprocessor communicates with the CPU through the PLC bus or with other devices through its serial interface. A typical example of an MCO in the PLC is SPECTO_S (see section B3 "Semigraphic Visualization").

MCO AS MAIN PROCESSOR IN A B&R MAESTRO SYSTEM

The B&R MAESTRO coprocessor can be operated in the slots that have been prepared especially for B&R MAESTRO components. They cannot be operated in slot 0 however, this slot is reserved for the PLC bus interface module MCIF2. If no MCIF2 is in the slot, a PLC module can be operated in slot 0.

RACK	SLOTS	SUITABLE FOR MCO
HCR166-0 (PLC/B&R MAESTRO)	16	$2 to $6
HCR169-0 (PLC/B&R MAESTRO)	16	$2 to $B

MFDD700 Floppy Disk Station

The MFDD700 is connected to the MCO hard disk. The file manager, the driver and several device descriptors are already programmed on the module PROM of the MCO hard disk.

MFDD70S Floppy Disk Station

If no MCO hard disk is used or if the floppy disk station must be mounted more than 2.5 meters (approx. 8 ft.) away, the serial disk station MFDD70S can be used. The only difference that can be noticed is that the data transfer is slower with the serial connection.

PLC Access

B&R MAESTRO coprocessors can access PLC peripherals in two different ways:

1. Software: This requires a function block in the PLC CPU for MCO communication.
   If no MCIF2 is in the slot or if data must be transferred consistently, data exchanged must be performed by means of software.

2. MCIF2: For time critical applications, the MCO can be accessed directly by running the MCIF2 PLC bus interface module in slot 0.

MULTIPROCESSOR SYSTEMS

If a single MCO is no longer sufficient for the application, you can set up a multiprocessor system. This consists of multiple MCOs. Since more processors can be accessed on a common bus, the technical aspects of the multiprocessor system hardware, such as bus accessing procedures, memory allocation and interrupt handling must be considered carefully during program development and organization.

Interrupt Master and MCO Master

If a system is equipped with one or more (max. 8), then an MCO must be assigned to take over the interrupt handling and the memory allocation as well as the functions of the MCO master. In this system, the interrupt master and the MCO master are the same unit. This master is automatically assigned by the boot program.

Bus Priority

When access to a common bus occurs simultaneously, collisions can happen. In order to organize the access on the bus, every MCO is assigned with a bus priority. The bus priority (0 to 7; 0 = highest priority) is automatically assigned by the boot program and displayed on the console terminal. The MCO and interrupt master always have the highest priority (0). The slots in the rack are arranged from left to right with increasing priority. The left-most MCO is always the MCO master and the right-most MCO always has the lowest priority.

Interrupt Distribution

Interrupts which are generated by B&R MAESTRO components (e.g. graphic or network controller), can only be acknowledged by the interrupt master (MCO Master). Because of this, every device driver must be loaded and initialized on the MCO master and on the respective MCO. Both drivers communicate during the initialization phase. The driver on the interrupt master knows which driver should actually process this interrupt. The device driver on the interrupt master transmits the interrupt from the periphery to the executing driver, which distributes the arriving interrupts to the individual MCOs.

Local and Global Addresses

There are local and global address areas in every MCO. The local address areas are situated in the memory of the respective MCO. Access to these address areas is very fast since only the local bus is required. The global address ranges are situated outside of the MCO and can be accessed by all MCOs. Access must therefore be controlled with bus access logic. Since this requires time, "wait states" are used.

All B&R MAESTRO Peripherals (e.g. graphic, networks) can be reached through the global bus. This supplies the user with all kinds of different possibilities but some discretion should be used. A worst case scenario could be that MCO A executes a program that is sitting in the application memory of MCO B or the other way around. That would mean that the MCOs were reading the instruction code of their programs via the global bus which considerably delays program execution. For this reason, programs should only be executed on the local bus of the MCO (local RAM, local ROM). Nevertheless, it is possible to transfer data between the MCOs and/or MAESTRO via global communication areas (data commons) or to load programs through the global bus into the memory without any noticeable delays.

MODEL NUMBERS AND DESCRIPTIONS

B&R MAESTRO coprocessors are delivered in sets. Three sets are available for every MCO:

- OEM System
- Development Kit, German
- Development Kit, English

Please ensure that the proper indicator code is entered with the model number (outer left-hand column).

B&R MAESTRO Coprocessor MCO1

Components	OEM System	Model Number
HCMCO1-A	MCO1 OS-9/68000 12.5 MHz, 512 KByte SRAM 16 Bit, FPU	**HCMCO:10AX**
SWMCO1-0	MCO1 System Software Diskette (driver and library)	

Components	Development Kit (German)	Model Number
HCMCO1-A	MCO1 OS-9/68000 12.5 MHz, 512 KByte SRAM 16 Bit, FPU	**HCMCO:10UD**
HCFP1024-0	Memory Expansion, 1 MByte Flash-PROM	
HCSYSC-TK	OS-9/Tool Kit, including ANSI C Compiler and Source Debugger	
SWMCO1-0	MCO1 System Software Diskette (driver and library)	
MAMSYS-0	B&R MAESTRO System Manual, German	
MAMCO-0	B&R MAESTRO Coprocessor Manual, German	
SWMTERM-0	B&R PC PROVIT 700 Emulation	

Components	Development Kit (English)	Model Number
HCMCO1-A	MCO1 OS-9/68000 12.5 MHz, 512 KByte SRAM 16 Bit, FPU	**HCMCO:10UE**
HCFP1024-0	Memory Expansion, 1 MByte Flash-PROM	
HCSYSC-TK	OS-9/Tool Kit, including ANSI C Compiler and Source Debugger	
SWMCO1-0	MCO1 System Software Diskette (driver and library)	
MAMAESTRO-E	B&R MAESTRO User's Manual, English	
MAMCO-E	B&R MAESTRO Coprocessor Manual, English	
SWMTERM-0	B&R PC PROVIT 700 Emulation	

Components	MCO1 Memory Expansion	Model Numbers
HCFP1024-0	MCO1 Plug-in Module 1,0 MByte Flash-PROM	**HCFP1024-0**
MAMSP-0	Memory Expansion Module User's Manual, German	**MAMSP-0**
MAMSP-E	Memory Expansion Module User's Manual, English	**MAMSP-E**

B&R MAESTRO Coprocessor MCO3

Components	OEM System	Model Number
HCMCO3-1A	MCO3 68030 MMU 33 MHz, 512 KByte SRAM, FPU 68882 2 MByte DRAM 32 Bit, 1 MByte FPROM, incl. OS-9 License	**HCMCO:31AX**
SWMCO3-0	MCO3 System Software Diskette (driver and library)	

Components	Development Kit (German)	Model Number
HCMCO3-1A	MCO3 68030 MMU 33 MHz, 512 KByte SRAM, FPU 68882 2 MByte DRAM 32 Bit, 1 MByte FPROM, incl. OS-9 License	**HCMCO:31UD**
HCSYSC-TK	OS-9/Tool Kit, Including ANSI C Compiler and Source Debugger	
SWMCO3-0	MCO3 System Software Diskette (driver and library)	
MAMSYS-0	B&R MAESTRO System Manual, German	
MAMCO-0	B&R MAESTRO Coprocessor Manual, German	
SWMTERM-0	B&R PC PROVIT 700 Emulation	

Components	Development Kit (English)	Model Number
HCMCO3-1A	MCO3 68030 MMU 33 MHz, 512 KByte SRAM, FPU 68882 2 MByte DRAM 32 Bit, 1 MByte FPROM, incl. OS-9 License	**HCMCO:31UE**
HCSYSC-TK	OS-9/Tool Kit, Including ANSI C Compiler and Source Debugger	
SWMCO3-0	MCO3 System Software Diskette (driver and library)	
MAMAESTRO-E	B&R MAESTRO User's Manual, English	
MAMCO-E	B&R MAESTRO Coprocessor Manual, English	
SWMTERM-0	B&R PC PROVIT 700 Emulation	

B&R MAESTRO Coprocessor MCO3MC

Components	OEM System	Model Number
HCMCO3MC-1A	MCO3 68030 MMU 33 MHz, 512 KByte SRAM, FPU 68882 10 MByte D RAM 32 Bit, PCMCIA IF, 1 MByte FPROM, OS-9	**HCMCO:32AX**
SWMCO3-0	MCO3 System Software Diskette (driver and library)	

Components	Development Kit (German)	Model Number
HCMCO3MC-1A	MCO3 68030 MMU 33 MHz, 512 KByte SRAM, FPU 68882 10 MByte D RAM 32 Bit, PCMCIA IF, 1 MByte FPROM, OS-9	**HCMCO:32UD**
HCSYSC-TK	OS-9/Tool Kit, Including ANSI C Compiler and Source Debugger	
SWMCO3-0	MCO3 System Software Diskette (driver and library)	
MAMSYS-0	B&R MAESTRO System Manual, German	
MAMCO-0	B&R MAESTRO Coprocessor Manual, German	
SWMTERM-0	B&R PC PROVIT 700 Emulation	

Components	Development Kit (English)	Model Number
HCMCO3MC-1A	MCO3 68030 MMU 33 MHz, 512 KByte SRAM, FPU 68882 10 MByte D RAM 32 Bit, PCMCIA IF, 1 MByte FPROM, OS-9	**HCMCO:32UE**
HCSYSC-TK	OS-9/Tool Kit, Including ANSI C Compiler and Source Debugger	
SWMCO3-0	MCO3 System Software Diskette (driver and library)	
MAMAESTRO-E	B&R MAESTRO User's Manual, English	
MAMCO-E	B&R MAESTRO Coprocessor Manual, English	
SWMTERM-0	B&R PC PROVIT 700 Emulation	